Claims

What is claimed is:

1. A non-volatile memory array for continuous simultaneous writing and erasing of data comprising:

a plurality of parallel word lines and a plurality of bit and programming lines, the word, bit, and programming lines configured to selectively apply bias voltages;

a multiplicity of memory cells aligned in rows between the word lines and receptive of said bias voltages, each memory cell having a non-volatile memory transistor and an adjacent current injector, the word lines having parallel poly plates in capacitive relation therewith with a portion of each poly plate carrying word line induced voltage to a memory transistor and to a current injector in different rows; and

whereby memory cells associated with a first row can be written to with word line voltage while memory cells in a second row can be simultaneously erased with the same voltage.

2. The apparatus of claim 1 wherein each non-volatile memory transistor is symmetrically paired with another non-volatile memory transistor.

3. The apparatus of claim 1 wherein current from the current injector flows to the memory transistor causing charged particle creation from impact ionization, the charged particles stored in the gate of memory transistor.

4. The apparatus of claim 3 wherein the current from the current injector is measured by an electrode having an applied bias.

5. The apparatus of claim 1 wherein each injector has a fast diode and a control transistor interacting at a sufficiently proximate range so as to cause impact ionization of charged particles some of which are stored in the memory transistor.

6. The apparatus of claim 1 wherein the non-volatile memory transistor and adjacent current injector are in side-by-side relation.

7. The apparatus of claim 6 wherein the non-volatile memory transistor and the adjacent current injector are separated by an isolation region.

8. The apparatus of claim 1 wherein each memory cell has at least two mutually connected floating gate transistors.

9. The apparatus of claim 1 wherein different rows of the memory array have different doping densities, thereby establishing different threshold voltages in different rows.

10. The apparatus of claim 9 wherein memory transistors of common thresholds are disposed in a row, with different rows having different thresholds.

11. The apparatus of claim 10 wherein different rows of memory transistors span a range of thresholds.

12. The apparatus of claim 1 wherein each memory cell is associated with an electrically communicating current meter measuring stored charge in the memory cell.

13. A non-volatile memory array comprising:

a plurality of memory cells arranged in rows and columns, each memory cell having a word line and a non-volatile memory transistor with source, drain and channel in a first isolation region of a substrate and an adjacent current injector in a second isolation region of the substrate and in space charge relation to the memory transistor, the second isolation region adjacent to the first isolation region, the space charge configured to accelerate to at least one of the source and drain of the memory transistor where impacts with the electrode give rise to energetic charged particles stored in the non-volatile memory transistor, the word line in capacitive relation to a poly plate having a first region forming a control gate for the memory transistor and having a second region forming a control means for the current injector.

14. The apparatus of claim 13 wherein rows of the array have word lines and columns have bit and program lines, all with selectively applied bias voltages, the word lines and poly plates of adjacent rows connected in a manner whereby memory cells in a first row can be selectively written to, simultaneously erasing of memory cells in an adjacent row.

15. The apparatus of claim 13 wherein different rows of the memory array have different doping densities, thereby establishing different threshold voltages in different rows.

16. The apparatus of claim 13 wherein memory transistors of common thresholds may be disposed in a row, with different rows having different thresholds.

17. The apparatus of claim 16 wherein different rows of memory transistors span a range of thresholds.

18. The apparatus of claim 13 wherein each memory cell is associated with an electrically communicating current meter measuring stored charge in the memory cell.

19. The apparatus of claim 13 wherein each memory cell has at least two mutually connected floating gate transistor.

20. A non-volatile memory array for continuous writing and reading of data comprising:

a plurality of parallel word lines and a plurality of perpendicular paired bit and program lines, the word, program, and bit lines configured to have selectively applied bias voltages;

a multiplicity of memory cells disposed in rows associated with the word lines, each memory cell having a transistor and an adjacent current injector, adjacent word lines having poly plates in capacitive relation with electrically communicating regions, extending from the

poly plates into the transistor and the current injector, whereby memory cells in a first row can be programmed as memory cells in a second row are erased.

21. A method of handling data in a non-volatile semiconductor memory array comprising:

writing data to at least one specified address in a first row in a non-volatile memory array; and

simultaneously erasing data at an address other than the specified address in a row adjacent to the first row in said array.

22. In a non-volatile transistor memory array, a semiconductor device comprising:

a word line extending linearly through a plurality of memory cells, and

a plurality of conductive plates in spaced apart, capacitive relation to the word line, each plate having a tang projecting from the plate and forming a gate for a transistor in a memory cell.

23. The device of claim 22 wherein each conductive plate is a polysilicon plate.

24. The device of claim 22 wherein a plurality of polysilicon plates are aligned over the word line in parallel relation therewith.

25. The device of claim 22 wherein a plurality of polysilicon plates are aligned under the word line in parallel relation therewith.

26. The device of claim 22 wherein the word line is a buried diffusion in a semiconductor substrate.

27. The device of claim 26 wherein said buried diffusion is a p+ diffusion in a n-well.

28. The device of claim 22 wherein each poly plate lies a tang forming a control gate of a memory transistor.

29. The device of claim 22 wherein each poly plate has a tang forming a control gate of an injector transistor, associated with a memory transistor.

30. The device of claim 22 wherein each poly plate has a first tang forming a control gate of a memory transistor and a second tang forming a control gate of an injector transistor associated with the memory transistor.

31. The device of claim 30 wherein the first and second tangs of each poly plate extend in opposite directions.

32. In a non-volatile transistor memory array of the type having a plurality of memory cells formed in and upon a semiconductor substrate, including capacitive elements having at least one capacitor plate, the improvement comprising:

a plurality of word lines, formed as a buried diffusion in the semiconductor substrate, with word lines positioned to be second capacitor plates to said capacitive elements of the memory cells.

33. The memory array of claim 32 wherein said word lines are under the capacitor plate of said capacitive elements.

34. The memory array of claim 32 wherein said word lines are parallel to each other.

35. The memory array of claim 32 wherein said word lines are p+ diffusions in n-wells.